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(54) APPARATUS AND METHOD FOR TRELLIS ENCODING DATA FOR TRANSMISSION IN DIGITAL DATA TRANSMISSION SYSTEMS

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(60) Division of application No. 08/895,612, filed on Jul. 16, 1997, now Pat. No. 6,307,868, which is a continuation-in-part of application No. 08/684,243, filed on Jul. 19, 1996, now Pat. No. 6,356,555, which is a continuation-in-part of application No. 08/588,650, filed on Jan. 19, 1996, now Pat. No. 5,793,759, which is a continuation-in-part of application No. 08/519,630, filed on Aug. 25, 1995, now Pat. No. 5,768,269, and which is a continuation-in-part of application No. 08/760,412, filed on Dec. 4, 1996, now Pat. No. 5,991,308.

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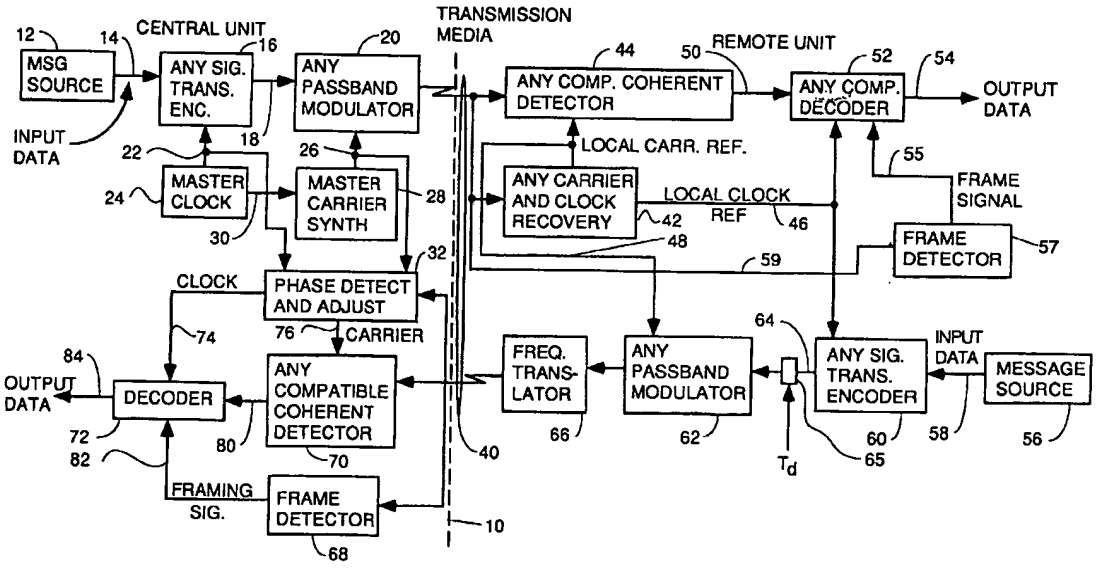
(57) ABSTRACT

A system for bidirectional communication of digital data between a central unit and a remote unit wherein the need for tracking loops in the central unit has been eliminated. The central unit transmitter generates a master carrier and a master clock signal which are used to transmit downstream data to the remote units. The remote units recover the master carrier and master clock and synchronize local oscillators in each remote unit to these master carrier and master clock signals to generate reference carrier and clock signals for use by the remote unit receiver. These reference carrier and clock signals are also used by the remote unit transmitters to transmit upstream data to the central unit. The central unit receiver detects the phase difference between the reference carrier and clock signals from the remote units periodically and adjusts the phase of the master carrier and master clock signals for use by the central unit receiver to receive the upstream data.



the
data being input to the filters. In other words, the error is multiplied by complex numbers representing the received chips which have had the signs of their Q or imaginary components inverted.

Detail Description Paragraph - DETX (381):
[0480] Training is performed immediately after ranging and periodically thereafter. If the insertion loss, phase response and group delay were known for the channel and the effects of dispersion on the pulse shapes were known, intersymbol interference could be effectively controlled by the **matched filters 761 in the CU receiver** of FIG. 31 and 570 in the RU transmitter of FIG. 33. However, even if these characteristics were known in advance, they tend to vary over time. Hence, in the preferred embodiment, an adaptive equalization process is performed to set variable coefficients in tapped delay line equalization filters to correct for the combined effects of residual distortion and noise caused by a dispersive and noisy channel. Prechannel equalization is performed in each RU and CU transmitter, and post channel equalization is performed in each RU and CU receiver in some embodiments. In the preferred embodiment, the training process is performed only for some filters in the system. Specifically, the CU precode equalization filter uses only averaged coefficients suitable for all RUs and the CE equalization filters in the RU receivers use only average coefficients found to be suitable for the average RU. Specific coefficients are computed for the SE circuits for each RU however after a training process similar to the process to be described below. This allows the equalized system to approach the ideal condition specified by the Nyquist criteria for distortionless transmission free of intersymbol interference so as to realize the full data carrying capacity of the channel. The adaptive equalization filters are tapped delay line filters in some embodiments with the tap delays equal to one chip time. In the preferred embodiment, the post channel filters are decision feedback equalizers. The equalization filters on both the transmit and receive side are embodied in precode equalization filter 563 in the transmitter of FIG. 32 and the FFE (feed forward) filter 764 and DFE (decision feedback) filter 820 along with least mean square calculation circuit 830 and difference calculating circuit 832 and FFE 765 in the receiver of FIG. 30.

prech eqd. post ch eqd

Scdma

Detail Description Paragraph - DETX (462):
[0561] Time alignment **phase shifts must be compensated** in this embodiment.

194 page

Detail Description Paragraph - DETX (475):
[0574] 1.3.3 Time alignment **phase shift compensation**

Claims Text - CLTX (25):
24. Th

nsmitter of FIG. 32 and the FFE (feed forward) filter 764 and DFE (decision feedback) filter 820 along with least mean square calculation circuit 830 and difference calculating circuit 832 and FFE 765 in the receiver of FIG. 30.

Detail Description Paragraph - DETX (462):
[0561] Time alignment **phase shifts must be compensated** in this embodiment.

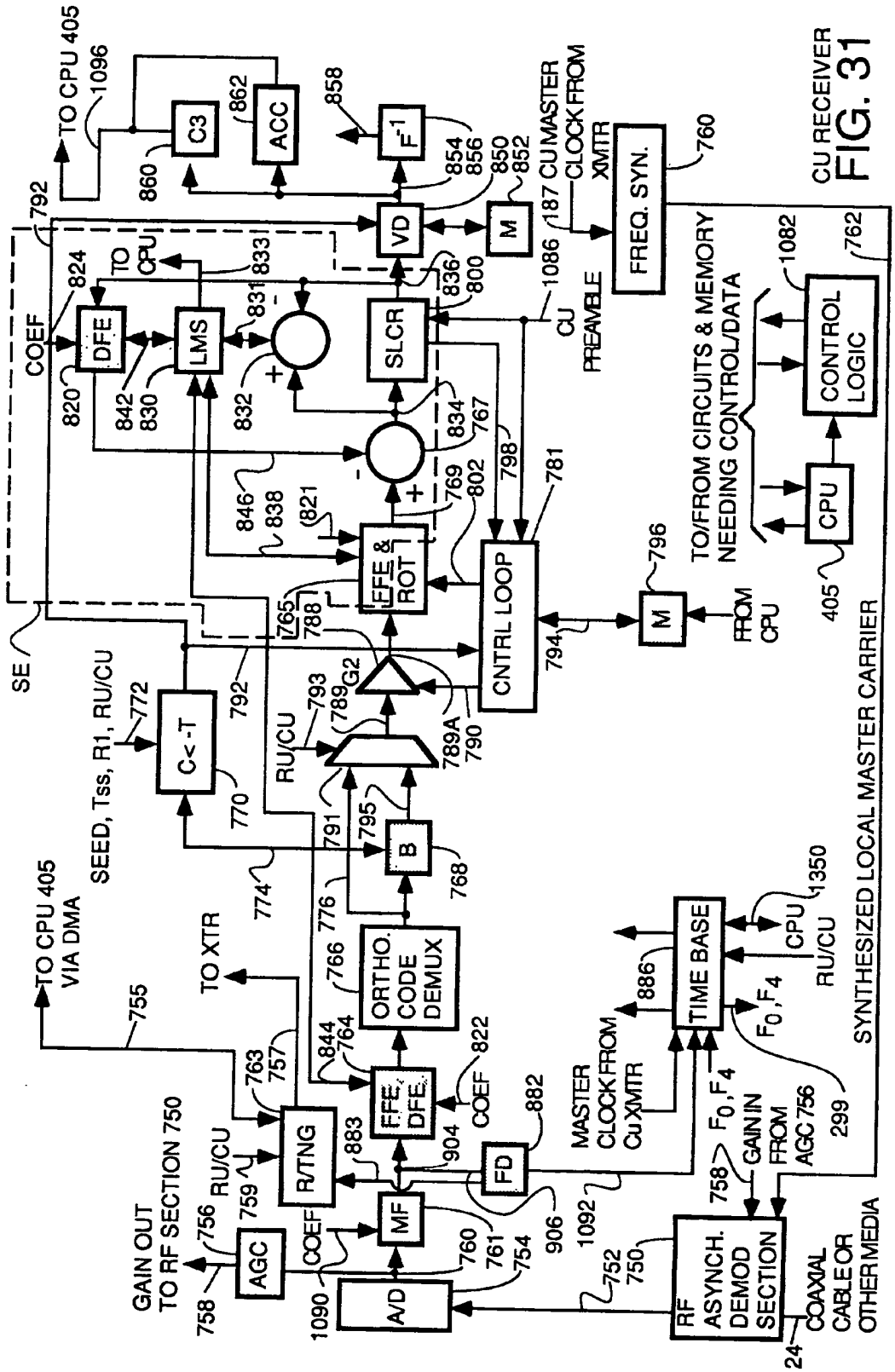
Detail Description Paragraph - DETX (475):
[0574] 1.3.3 Time alignment **phase shift compensation**

Claims Text - CLTX (25):
24. The apparatus of claim 20 wherein said remote unit transmitter includes a precode equalization filter in the form of a digital FFE filter having multiple coefficients, and wherein said remote unit transceiver includes circuitry for receiving command and control communications from said central unit transceiver instructing changes in the value of said delay T.sub.d and for multiplying the coefficients of said FFE filter in said remote unit transmitter by the negative of the phase shift at said central unit transceiver of signals received from this remote unit transceiver which will be caused by the change in the delay T.sub.d at said remote unit transceiver for subsequent transmissions so as to provide **phase shift compensation**.

Claims Text - CLTX (26):
25. The apparatus of claim 21 wherein said remote unit transmitter includes a precode equalization filter in the form of a digital FFE filter having multiple coefficients, and wherein said remote unit transceiver includes circuitry for receiving command and control communications from said central unit transceiver instructing changes in the value of said delay T.sub.d and for multiplying the coefficients of said FFE filter in said remote unit transmitter by the negative of the phase shift at said central unit transceiver of signals received from this remote unit transceiver which will be caused by the change in the delay T.sub.d at said remote unit transceiver for subsequent transmissions so as to provide **phase shift compensation**.

Claims Text - CLTX (27):
26. The apparatus of claim 22 wherein said remote unit transmitter includes a precode equalization filter in the form of a digital FFE filter having multiple coefficients, and wherein said remote unit transceiver includes circuitry for receiving command and control communications from said central unit transceiver instructing changes in the value of said delay T.sub.d and for multiplying the coefficients of said FFE filter in said remote unit transmitter by the negative of the phase shift at said central unit transceiver of signals received from this remote unit transceiver which will be caused by the change in the delay T.sub.d at said remote unit transceiver for subsequent transmissions so as to provide **phase shift compensation**.

Claims Text - CLTX (28):
27. The apparatus of claim 23 wherein said remote unit transmitter includes a precode equalization filter in the form of a digital FFE filter having multiple coefficients, and wherein said remote unit transceiver includes circuitry for receiving command and control communications from said central



SDMA controlled by the match filters 761 in CU Fig 31 570 in RU in xmtr

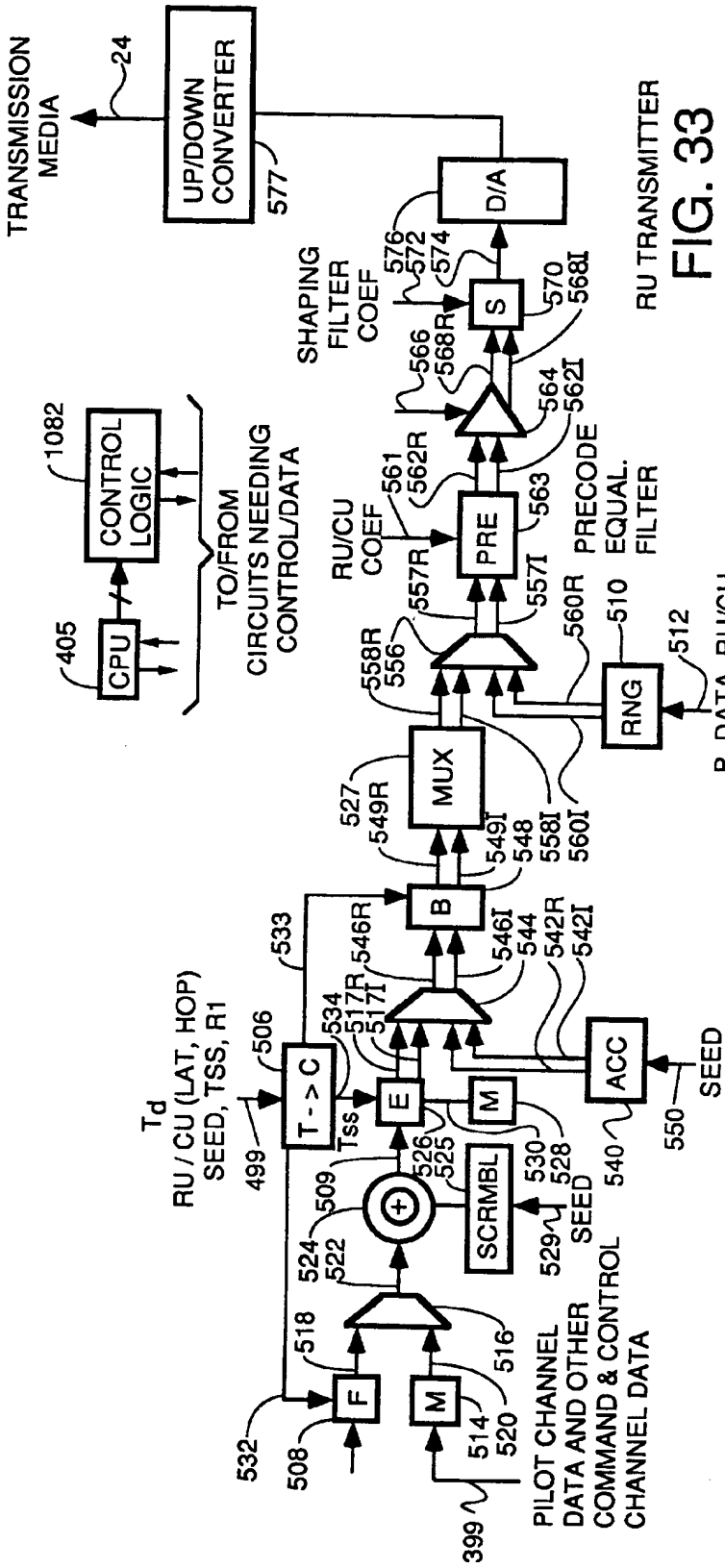

TRANSMISSION MEDIA
24
UP/DOWN CONVERTER
577
D/A
576
572
574
SHAPING FILTER COEF
S
570
568I
566
568R
564
562I
562R
561
RU/CU COEF
PRE
563
557I
557R
PRECODE EQUAL. FILTER
RU TRANSMITTER
1082
CONTROL LOGIC
405
CPU
TO/FROM CIRCUITS NEEDING CONTROL/DATA
558R
556
560R
510
512
RNG
P, DATA, RU/CU
MUX
527
549R
549I
548
558I
560I
B
546R
546I
544
542R
542I
533
534
517R
517I
506
T -> C
Td
RU/CU (LAT, HOP) SEED, TSS, R1
499
Tss
E
M
ACC
550
SEED
526
525
530
528
SEED
540
509
SCRMBL
529
524
522
518
516
F
M
532
508
514
520
399
PILOT CHANNEL
DATA AND OTHER
COMMAND & CONTROL
CHANNEL DATA

FIG. 33

11):

[0120] The baseband signal is received and processed by any compatible decoder represented by block 52. The function of decoder 52 is to reverse the encoding and/or multiplexing process carried out by encoder 16 at the central unit transmitter and determine which symbol was sent during every chip time or bit time. The decoder 52 receives the local clock signal on line 46 and uses it to determine when the bit time or chip time boundaries are for purposes of sampling. The decoder 52 also functions to detect the frame boundaries of the downstream frames and reorganize the received data back into the frames organized by the encoder 16 for output on bus 54. To assist the decoder is doing the frame boundary recognition, a framing signal is generated on line 55 by a frame detector circuit 57. Any prior art decoder design that can perform this function for the particular encoding/multiplexing scheme selected for use by the central unit transmitter will suffice to practice the invention. The frame detector circuit 57 receives the downstream RF signal on line 59 (or is coupled to the baseband signal output from the detector 44) and looks for unique frame boundary signals in the stream of data transmitted from the central unit transmitter. Frame detectors are well known in the art, and there is such a circuit in every digital communication system that transmits data in frames. One method of frame detection used in the SCDMA examples presented below is separation of frames by a guardband, and transmission of a unique Barker code by the central unit transmitter during every guardband. This stream of incoming data at the remote **receiver is passed through a filter having a transfer function matched** to said Barker code and the correlation peak which results when the Barker code passes through the matched filter is used to mark the frame boundaries.

09/10/033,799

SCDMA

RU filter has xfer function matched to Barker code RCVd

RCV FIR match
XMT FIR

Detail Description Paragraph - DETX (79):

[0182] The CU next instructs the RU to entering an equalization training interval to determine the coefficients to set into the RU **transmitter's precode filter to predistort** the RU signals to eliminate channel distortion and test the quality of the ranging result. The training algorithm is discussed below, but other ways of performing equalization which are known in the prior art can also be used. In addition, other ways of achieving frame synchronization known in the prior art can also be used and other ways of achieving synchronization of the RU local carrier oscillator and local clock oscillator to the master carrier and master chip clock signals, respectively, known in the prior art can also be used to practice the invention of eliminating tracking loops in the CU in the SCDMA environment.

predistort RU xmtter

Detail Description Paragraph - DETX (91):

[01

s in the CU
in the SCDMA environment.

Detail Description Paragraph - DETX (91):

[0194] The fine tuning mode is represented by the process of block 202. In this process, the CU instructs the RU which has aligned itself in the gap on how to adjust its delay vector in order to center the correlation peak calculated by the CU to the exact middle of the gap. In the preferred embodiment, the gap is comprised of 16 chips which comprise 8 chips in the middle of the gap and then 4 chips on either side of this middle group of 8. It is desirable during the fine tuning mode to get the correlation peak centered in the middle of the middle 8 chips. As mentioned above, a chip is a small interval of time equal to the frame period of 125 microseconds divided by the 448 chips which comprise each frame. In other words, each chip is 279 nanoseconds in duration. The fine tuning process of block 202 involves sending messages back and forth between the CU and the RU which has been identified as having aligned itself in the gap. These messages are sent over the management and control channels. Since clock recovery and carrier recovery has already been accomplished in the RUs before ranging is started, receiving of these management and control messages is no problem and constellations involving phase information can be used. In some embodiments, the exchange involves only one instruction from the CU to the RU saying, for example, "Increase your delay vector by 2 chips" or , "Decrease your delay vector by 3 chips". In other embodiments, multiple trial and error adjustments are made. The RU then makes the instructed adjustment and retransmits the Barker code. The CU again calculates a correlation peak and examines where the peak occurs in the gap. If the peak occurs in a suitable position, the CU sends a message to the RU telling it to stop adjusting its delay vector as satisfactory alignment has been achieved. The RU then adjusts the coefficients of its precode equalization filters 563 in FIG. 33 to **compensate for the phase** change caused by the time alignment shift of the fine tuning process. This is done by multiplying all four feed forward coefficients by the negative of the phase shift caused by the timing offset.

Detail Description Paragraph - DETX (249):

[0350] In acquisition mode, the

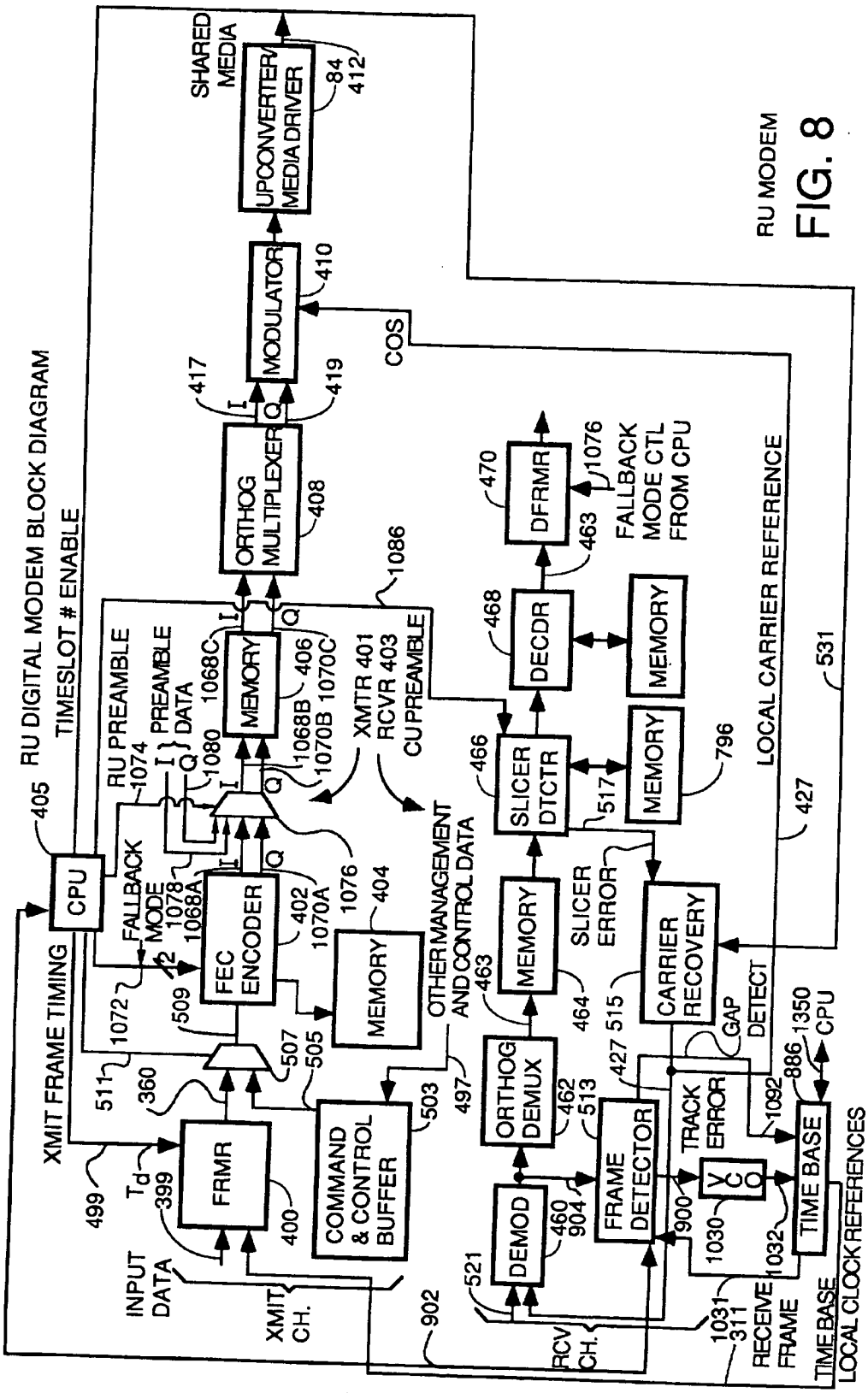

RU DIGITAL MODEM BLOCK DIAGRAM
RU MODEM
SHARED MEDIA
UPCONVERTER MEDIA DRIVER
84
412
MODULATOR
410
COS
ORTHOG MULTIPLEXER
408
417
419
I
Q
DFRMR
470
1076
FALLBACK MODE CTL FROM CPU
463
DECDR
468
MEMORY
1086
XMTR 401
RCVR 403
CU PREAMBLE
RU PREAMBLE
1074
PREAMBLE DATA
1080
1068C
406
1068B
1070C
1070B
405
CPU
TIMESLOT # ENABLE
XMIT FRAME TIMING
FALLBACK MODE
1078
1068A
FEC ENCODER
402
1070A
1076
404
MEMORY
OTHER MANAGEMENT AND CONTROL DATA
SLICER DTCTR
466
517
796
LOCAL CARRIER REFERENCE
531
427
SLICER ERROR
463
MEMORY
464
CARRIER RECOVERY
515
GAP DETECT
1350
CPU
886
1092
TRACK ERROR
427
513
ORTHOG DEMUX
462
497
503
COMMAND & CONTROL BUFFER
507
505
509
1072
511
360
499
T_d
399
FRMR
400
INPUT DATA
XMIT CH.
902
DEMOD
460
904
521
FRAME DETECTOR
900
1030
Y
C
O
1032
TIME BASE
1031
311
RECEIVE FRAME
TIME BASE
LOCAL CLOCK REFERENCES
RCV CH.

FIG. 8

APPARATUS AND METHOD FOR TRELLIS ENCODING DATA FOR TRANSMISSION IN DIGITAL DATA TRANSMISSION SYSTEMS

[0001] This application is a continuation-in-part application of U.S. patent application Ser. No. 08/684,243, filed Jul. 19, 1996, invented by Shlomo Rakib and Yehuda Azenkot which was a continuation-in-part application of U.S. patent application Ser. No. 08/588,650, filed Jan. 19, 1996, invented by Shlomo Rakib and Yehuda Azenkot, which was a continuation-in-part application of U.S. patent application Ser. No. 081519,630, filed Aug. 25, 1995, invented by Shlomo Rakib and Yehuda Azenkot, now U.S. Pat. No. _____, issued _____, the contents of all of which are hereby incorporated by reference. This application is also a continuation-in-part application of a U.S. patent application entitled LOWER OVERHEAD METHOD FOR DATA TRANSMISSION USING ATM AND SCDMA OVER HYBRID FIBER COAX CABLE PLANT, Ser. No. 08/760,412, filed Dec. 4, 1996, invented by Amir Fuhrmann, Shlomo Rakib and Yehuda Azenkot, now co-pending, the entirety of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The invention pertains to the field of bidirectional passband digital communication systems, and, more particularly to the field of improvements in head end or central office modems to remove the phase locked loops therefrom.

[0003] Digital data communication systems are well known in the art. Many treatises are available that describe them. Among these treatises are: Dixon, *"Spread Spectrum Systems with Commercial Applications"*, Third Edition, 1994 (Wiley & Sons, New York) ISBN 0 471 59342-7; Stallings *"Data and Computer Communications"*, 4th Ed. 1994 (Macmillan Publishing Co., New York) ISBN0-02-415441-5; Lee and Messerschmit, *"Digital Communication*, 2d Ed.", 1994 (Kluwer Academic Publishers, Boston), ISBN 0 7923 9391 0; Haykin, *"Communication Systems"* Third Edition 1994 (Wiley & Sons) ISBN 0 471 57176-8; Elliott, *Handbook of Digital Signal Processing: Engineering Applications*, (Academic Press, Inc. San Diego, 1987), ISBN 0-12-237075-9, all of which are hereby incorporated by reference. Generally, the problem which the invention is an attempt to solve is how to get rid of as many continuous tracking loops as possible in a bidirectional digital data communication system. The reasoning for this can be understood from the following discussion.

[0004] Digital data distributed communication systems can be baseband systems or passband systems. In baseband systems, the transmission media has the capability of transmitting digital pulses between widely separated transmitter and receiver locations. Passband systems require that the digital data be modulated onto a carrier frequency for transmission over the media.

[0005] Receivers for digital data passband systems can be either coherent or noncoherent. In coherent systems, the receiver has a local oscillator, usually taking the form of a phase locked loop (PLL) which is part of a continuous tracking loop and is maintained in constant phase lock with the phase and frequency of the carrier on which the received data is modulated. Coherent systems can make use of modulation schemes which alter either the phase, frequency or amplitude or any combination thereof of the carrier in accordance with the information content of the digital data to be transmitted. Incoherent systems do not have the local oscillator at the receiver phase locked to the carrier phase and frequency. In these systems, the designers have chosen to ignore the phase of the received signal at the expense of some degradation of the system performance and throughput.

[0006] Coherent systems can utilize binary or M-ary amplitude shift keying (ASK), phase shift keying (PSK) or frequency shift keying (FSK), as well as M-ary amplitude phase keying (APK) of which QAM (quadrature amplitude modulation) is a special case. Incoherent systems are limited to binary or M-ary ASK, FSK or differential phase shift keying (DPSK).

[0007] Coherent systems are higher performance systems because they have an additional degree of freedom for use in the modulation scheme which means more complex constellations of symbol sets can be used and more data bits can be encoded in each symbol in the constellation. This translates to greater throughput.

[0008] However, coherent systems are more complex since they require additional tracking loop circuitry at the receiver to recover the transmitted carrier and use the information so derived to steer the local oscillator so as to maintain its phase and frequency locked to the phase and frequency of the carrier. Usually the local oscillator being steered in the receiver is a PLL or has a voltage controlled oscillator negative feedback system in it (which is at the heart of almost every tracking loop). Carrier synchronization has been achieved by any one of a number of different ways in the prior art including use of PLLs where the carrier is not suppressed or Mth power tracking loops or Costas tracking Loops where the carrier is suppressed. Mth power and Costas tracking loops also contain voltage controlled oscillators as part of the tracking loop. The problem is that PLLs and negative feedback voltage controlled oscillators in tracking loops can and often do lose lock especially where there is rapid change in phase or frequency caused by conditions in the transmission media. When a PLL or other tracking loop loses lock, the system goes out of synchronization and fails to communicate data—its sole purpose in life.

[0009] All digital data communication also requires clock synchronization in the receiver to the clock in the transmitter because data is sent during discrete times. These discrete times are variously called chip times, bit times or symbol times in the prior art references. The importance of synchronization of the clock in the receiver to the clock in the transmitter is that in all forms of modulation, the amplitude, phase or frequency of the carrier (or some combination of these) must be sampled during each chip time so as to determine which symbol in the alphabet or code set in use was transmitted during that chip time based upon the phase, amplitude or frequency characteristics of the carrier during that chip time.

[0010] Receiver clock synchronization can be done on either a long term basis or a short term basis. Short term clock synchronization is called, amazingly enough, asynchronous transmission, but in fact the receiver clock is periodically synchronized to the transmitter clock at the beginning of transmission of each "character". A character is a collection of 5 to 8 symbols which are transmitted over a

very short time (usually the symbols or binary bits that only have two states). The receiver clock resynchronizes during each character at the beginning thereof and need not resynchronize until the next character starts. Asynchronous transmission is cheap and less complex since timing synchronization problems caused by transmission of long uninterrupted streams of bits is avoided by sending the bits one character at a time and requiring synchronization between the receiver clock and transmitter clock only during that character.

[0011] The problem with asynchronous transmission is the high overhead. Each character of 5 to 8 bits must include a start bit, 1 or 2 stop bits and a parity bit. The start bit is used by the receiver to resynchronize its clock. The overhead of 2-3 bits per character of 5-8 bits makes asynchronous transmission inefficient to transmit large volumes of data. Asynchronous transmission can be extended to sending several characters grouped together with a preamble which is long enough for the receiver to synchronize to transmitted before every group of characters and a tracking loop to maintain the receiver clock in synchronization with the transmitter clock during the transmission of the group of characters. The concepts of the invention are applicable to asynchronous transmission where there is a tracking loop in the remote unit receiver but no tracking loop in the central unit receiver and only a periodic or occasional phase adjustment of the master clock and master carrier phase for use by the central unit receiver.

[0012] Synchronous transmission is a more efficient way of transmitting data since blocks of symbols or bits can be transmitted without start and stop codes. Sampling by the receiver during the middle of each bit or chip time is accomplished by keeping the receiver clock in synchronization with the transmitter clock. This maintenance of clock synchronization has been done in the prior art in many different ways. For example, a separate clock line can connect the transmitter and receiver, but this is impractical in many situations. A way of avoiding this is to embed the clock information in the data signal transmitted from the transmitter and recover the clock in the receiver.

[0013] Clock recovery has been done in a number of different ways in the prior art including transmitting the clock along with the data bearing signal in multiplexed form and using appropriate filtering of the modulated waveform to extract the clock. Another method is to use a noncoherent detector to first extract the clock and then processing the noncoherent detector output to recover the carrier. Where clock recovery follows carrier recovery, the clock is recovered from demodulated baseband signals. The early-late gate symbol synchronizer has also been used in the prior art to synchronize the receiver clock to the transmitter clock. This type clock recovery takes advantage of the fact that a matched filter output of a filter matched to a rectangular clock pulse is a triangular waveform which can be sampled early before the peak and late after the peak. By changing the timing of the sampling until the early and late samples have equal amplitude, the peak of the matched filter output signal can be found, and this will have a fixed phase relationship to the clock phase. This information is then used to steer a voltage controlled oscillator in a negative feedback system. Again, complicated circuitry centered around a voltage controlled oscillator is needed to recover the clock.

[0014] A technique called remote loopback or remote clock has been used in the prior art on, for example T1 type digital data communication phone lines. This technique is similar to the aspect of the invention involving having the remote unit local clock synchronized to the central unit master clock and using that local clock at the remote unit receiver for the remote unit transmitter. It is also similar to the aspect of the invention of using the central unit master clock, after adjustment in phase to synchronize it to the phase of the received clock from the remote unit transmitter, as the clock signal from the central unit receiver.

[0015] Since PLLs and tracking loops are not always reliable, and add complication and expense to receivers, it is desirable to be able to get rid of them wherever possible. Thus, a need has arisen for a bidirectional digital communication system where continuous tracking loops in the central unit receiver (or the receiver in the unit having the transmitter which transmits with the master clock and master carrier signals) have been eliminated.

SUMMARY OF THE INVENTION

[0016] A bidirectional digital data communication system according to the teachings of the invention will have: a central unit transmitter with any encoder to receive downstream data, encode it and drive any type of digital passband modulator with the encoder receiving a master clock signal from a master clock oscillator and the modulator receiving a master carrier oscillator; a remote unit receiver which has any compatible detector which receives a local carrier reference signal which is synchronized in frequency and phase to the master carrier signal and which is generated by any form of carrier recovery circuit, with the detector driving a decoder to decode the received data and output it, with the decoder receiving a local clock signal which has been synchronized with the transmitter master clock signal by any clock recovery circuit; a remote unit transmitter having any encoder type for receiving upstream data, encoding it and driving any digital passband modulator, the encoder receiving the local clock reference generated by the remote unit receiver clock recovery circuit and the modulator receiving the local carrier reference signal generated by the remote unit carrier recovery circuit; and a central unit receiver with any compatible coherent detector to detect the signal transmitted from the remote unit transmitter, with the central unit detector using the central unit master carrier from the master carrier oscillator in the transmitter but adjusted in phase to account for propagation delay from the remote unit, and with the decoder using the master clock signal from the central unit transmitter master clock oscillator but adjusted in phase for the propagation delay from the remote unit to the central unit. Thus, the central unit has no phase locked loops or other voltage controlled oscillator circuits for clock recovery or carrier recovery.

[0017] In the preferred embodiment, the master carrier and master clock are recovered in the RUs and used to transmit data upstream along with preamble data preceding payload data. The preamble data from each RU is used by the central unit transceiver to generate an amplitude and phase correction factor for that RU. The signals from that RU are then demodulated using the CU master carrier and demultiplexed and detected using the CU master clock. Phase and amplitude errors in the detection process caused by latency and channel impairments are eliminated or reduced by using the

phase and amplitude correction factors developed for this RU from its preamble data. Thus, there is no need for continuous tracking loops in the CU receiver to recover the clock and carrier used by each RU to transmit its data. This single master carrier and master clock concept and the frame synchronization provided by ranging, and the improved throughput and lower error rates provided by the equalization and power alignment processes taught herein are useful in any form of bidirectional digital data distributed communication system regardless of the form of encoding, multiplexing or modulation used. Examples of the types of multiplexing that can be used in such systems are CDMA, TDMA, inverse Fourier, DMT or any other system where orthogonal signals are used to encode each separate channel of data from a source such as sine and cosine signals etc.

[0018] In the broadest embodiment of the invention involving no continuous tracking loops in the CU receiver to recover RU clock and carrier, the type of central unit transmitter and modulation scheme is not important nor is it important whether the central unit transmits a single channel of digital data downstream or multiplexes several channels. If the central unit transmitter is a multiplexing transmitter, the type of multiplexing is not important. Likewise, the type of detector used in the remote unit receiver is not important as long as it is compatible with the modulation scheme in use and it is not critical whether the central unit transmitter transmits the master carrier or suppresses it or transmits the master clock separate or embeds it in the data so long as the master clock and carrier phase information get transmitted somehow to the RUs such as embedded in the Barker code of the preferred embodiment. Likewise, the type of carrier recovery and clock recovery circuits used in the remote unit to synchronize the local clock and local carrier oscillators to the master clock and master carrier are not critical. Also, the type of decoder used in the remote unit receiver is not critical so long as it is compatible with the type of encoder used at the central unit transmitter. For the remote unit transmitter, any type of encoder and any type of modulator may be used for the upstream data, and the type of encoding and the type of multiplexing, if any, used for the upstream direction need not be the same as the downstream direction. The clock and carrier signals used by the remote unit transmitter are the same clock and carrier signals used by the remote unit receiver.

[0019] The central unit receiver can use any type of detector that is compatible with the modulation scheme used by the remote unit transmitter. Likewise, the type of decoder used in the central unit receiver is not critical so long as it is compatible with the remote unit transmitter encoder. The structure and operation of the central unit receiver phase detection and adjustment circuit is not critical to the invention. The only requirement on this circuit is that it be able to occasionally or periodically detect any phase differential between the central unit master carrier and the carrier used to transmit by the remote unit transmitter and detect any phase difference between the central unit master clock and the clock information used to transmit the received data. These phase differences are used by the central unit receiver to occasionally or periodically adjust the phase of the master clock and master carrier to match the phases of the carrier and clock signals used by the remote unit transmitter as received at the central unit receiver.

[0020] The invention is applicable to both asynchronous and synchronous methods of transmission, although synchronous transmission is much more efficient in terms of overhead consumed per unit of payload data delivered. Use of the invention in asynchronous transmission will be useful in asynchronous systems where tracking loops are used to maintain synchronization of the remote unit receiver local clock during transmission of one or more characters in a group.

[0021] In the preferred embodiment, the transmitters of the RU use synchronous code division multiplexing (SCDMA). SCDMA is defined as transmission of frames of spread spectrum signals with data from different channels spread using orthogonal pseudorandom spreading codes, said frames being synchronously transmitted from different RUs located at diverse locations such that all frames of corresponding frame number from all RUs arrive at the CU modem with their frame boundaries exactly aligned in time with the frame boundaries of the CU frame of the same frame number. The upstream data is then demultiplexed and decoding by the inverse code transformation that was used in the RU transmitter to spread the spectrum of the data using the orthogonal, pseudorandom spreading codes.

[0022] According to the most preferred embodiment, there is provided a code division multiplexing multiple access (CDMA) scheme using orthogonal codes to encode multiple channels of digital data for simultaneous transmission over a cable television media which is also carrying frequency division multiplexed cable television programming.

[0023] Further, in this most preferred embodiment, alignment of multiple subscriber remote units at diverse locations on the cable television media to the same frame alignment reference is used to substantially reduce crosstalk between adjacent codes and allow multiple users to simultaneously share the same cable TV media for auxiliary services other than cable TV programming delivery. The ranging process described herein is useful for any digital communication system which delivers data from physically distributed transmitters to a central location in frames, but in the context of a CDMA system on a cable TV plant, it provides for synchronous CDMA which greatly increases system payload capacity. The use of synchronous CDMA coupled with frequency division multiplexing of upstream and downstream data on different frequencies than the cable TV programming provides a system whereby the entire bandwidth devoted to the digital auxiliary services may be simultaneously shared by multiple users who share a plurality of channels. Any of the known ways of achieving frame alignment may be used to achieve synchronous code division multiple access data transmission. In the preferred embodiment, frame alignment is achieved with the bulk of the processing done by the RUs with the CU only acting in a passive role as a sensor for deciding if a Barker code is in the gap, if there is more than one Barker code in the gap, asking for authentication and providing feedback for all of the above and for fine tuning processing to exactly center each RU's Barker code in the gap. This ranging process is done by alignment of ranging signals transmitted by remote units to guardbands or gaps between frames.

[0024] One inventive concept disclosed herein is to achieve high noise immunity by spreading the energy of the transmitted data out over time during transmission, and then

compressing the energy again at the receiver to recover the data. Spreading the energy of the transmitted data out over time reduces susceptibility to burst errors and impulse noise. In addition to this spreading concept, the spectral efficiency of the system is enhanced by transmitting multiple separate channels of data over the same media without interference by using separate orthogonal codes to encode the data of each channel so that no interference results when all channels are simultaneously transmitted so long as proper frame alignment is maintained. In this way, the spectral efficiency, i.e., a measure of the amount of data that can be sent from one place to another over a given bandwidth, is enhanced without degradation of the data by crosstalk interference. The orthogonality of the codes used for each data stream, i.e., each channel or conversation, minimizes crosstalk between channels where the system is properly aligned, i.e., synchronized.

[0025] Using cyclic, orthogonal codes for SCDMA further enhances noise abatement by providing the ability to perform equalization using a subset of these codes. Equalization, as that term is used herein, refers to the process of determining the amount of crosstalk between adjacent codes resulting from minor errors of frame timing alignment and then generating phase and amplitude correction factors which can be used to negate the crosstalk. In the preferred embodiment, the orthogonal codes are cyclic codes.

[0026] In some species within the genus of the invention, code diversity is used to achieve further noise immunity. It has been found that some orthogonal codes are less immune to narrow band interference and other sources of noise than others. To avoid using such codes to spread the data from the same channel or timeslot all the time, code hopping is used in these preferred species of the inventive genus. Code diversity is achieved in several different ways, but, in the preferred embodiment, each transmitter uses a code shuffler circuit and each receiver uses a code deshuffler circuit. All shuffler and deshuffler circuits receive the same seed and generate the same sequence of pseudorandom numbers therefrom. These pseudorandom numbers are used to generate read pointers to a framer memory and write pointers to a buffer memory. The framer memory is where the information vectors or symbols are stored, and the read pointers generated by the shuffler circuits are used to read the timeslot data, i.e., symbol/information vector elements out in pseudorandom fashion and store them in a buffer in accordance with the write pointers generated by the code hopping shuffler circuit. The information vector elements thus stored in the buffer are used to do the matrix multiplication required by the code division multiplexing scheme. Alternatively, the symbol elements may be read out sequentially from the framer memory and stored pseudorandomly in the buffer.

[0027] The effect of this synchronous CDMA scheme is to "whiten" the noise sources such that no matter how complex the noise signals, the noise can be effectively managed using conventional error detection and correction bits in a forward error correction scheme. The digital data providing the interactive or bidirectional data communication is sent using a CDMA scheme, but for purposes of synchronization, the CDMA scheme is mixed with a TDMA scheme. More precisely, a guardband or gap which is free of data is added between frames of the CDMA signal. Digital data is transmitted in frames, each frame comprising 3 data symbols and a guardband. The guardband is used for non-data usage such as ranging, alignment and equalization.

[0028] The synchronous CDMA modulation scheme disclosed herein may be used with any shared transmission media and with any apparatus or method that can get all remote units synchronized to the frame timing of the central unit including the ranging/alignment scheme disclosed herein. Other possible methods of synchronizing to the same frame timing are for all remote units and the central unit to receive the same timing reference signals from some source such as internal atomic clocks or from an external source such as a Global Positioning System satellite from which all remote units and the central unit are effectively equidistant.

[0029] Likewise, the ranging/alignment scheme disclosed herein is useful for any other modulation scheme which transmits digital data in frames, requires frame synchronization and can insert a guardband between the frames.

[0030] Some species within the inventive genus use M-ary modulation code division multiplexing. Each remote unit receives a time division multiplexed stream of digital data. Each timeslot contains 9 bits of data. Each 9 bits is stored in a framer memory, and is divided into three tribits, each having 3 bits during readout of the memory. Each of the three symbols transmitted each frame is comprised of 144 of these tribits, one for each timeslot or channel. These tribits are encoded with a 4th bit prior to spreading by the code division multiplexing operation. The 4th bit is added by a Trellis forward error correction encoder to each tribit based upon the three bits of the tribit and based upon the previous state for this timeslot's data during the last frame. This 4th bit adds sufficient redundancy to enable a Viterbi Decoder in the central unit receiver to make a more error free determination of what data was actually sent in the presence of noise without requesting retransmission. The 4th bit also maps each tribit to a 16 point QAM (quadrature amplitude modulation) constellation by using the first two bits to represent the inphase or I axis amplitude and the last two bits to represent the quadrature or Q axis amplitude. Thus, M-ary modulation is used to achieve greater spectral efficiency.

[0031] With the system described herein, full 10 megabit/second traffic volume per each 6 MHz channel can be achieved in both the upstream and downstream direction over HFC. Unlike conventional CDMA, SCDMA transmission from transmitters like those disclosed herein stays within 6 MHz bands that do not interfere with or effect other adjacent channels. SCDMA has a number of other advantages over pure FDMA and TDMA systems in terms of capacity, scalability and bandwidth allocation. Standard IS-95 asynchronous Code Division Multiple Access spread spectrum systems are hindered by the capacity constraints of the 5-40 MHz upstream channel and the presence of a large amount of noise, and they often require 30 MHz wide channels which creates channel interference problems with neighboring services in the HFC spectrum. The biggest problem with asynchronous CDMA systems is self-generated noise because the RUs are not aligned with each other thereby losing orthogonality and creating a high degree of mutual interference. The higher self-generated noise raises the noise floor and reduces the capacity. SCDMA system insure that the RUs are in frame synchronization with each other and using orthogonal codes to minimize mutual interference as data is sent upstream. Preferably, SCDMA trans-

mitters are also used to send data downstream. With the system described herein, multiple streams of digital data, each having a 64 kbps throughput can be simultaneously sent over a 6 MHz channel with a total 10 Mbps throughput. Each data stream is Trellis encoded, interleaved and spread over the entire 6 MHz using its own individual spreading code. Use of forward error correction and interleaving increases noise immunity to impulse noise, narrowband interference and Gaussian noise. The Trellis coding adds 4.8 dB coding gain, and interleaving enables withstanding long duration impulse noise of up to 100 microseconds without incurring errors. Use of spread spectrum technology adds another 22 dB processing gain. The combination of techniques yield a total 27 dB interference rejection allowing the system to operate in negative Carrier to Noise Plus Interference Ratio. The SCDMA transmitters are combined with TDMA payload data input streams which makes the system extremely scalable.

[0032] The high capacity of the SCDMA system disclosed herein is made possible by orthogonality which is made possible by the orthogonality of the spreading codes which is a result of the ranging process and the equalization process. The ranging process assures frame synchronization such that all codes arrive from distributed RUs arrive at the CU at the same time. The ranging process is carried out periodically to account for cable expansion/contraction with changing temperature, but the process is transparent to payload traffic in that it does not slaw it down, stop it or cause errors. Re-ranging occurs upons certain error conditions and upon disconnect from the network and each powerup.

[0033] Equalization is achieved by measuring the channel response from each user to the CU and adjusting a precoder at the RU transmitter to "invert the channel", i.e., predistort the transmitted signal such that it arrives undistorted at the CU. Power alignment by each RU such that each RU transmission reaches the CU at approximately the same power level also helps to minimize mutual interference.

[0034] Dynamic bandwidth allocation allows as many 64 kbps streams or channels as necessary to be allocated to a particular service so that high demand applications such as video teleconferencing or high speed internet access can be supported simultaneously with low demand applications like telephony over the same HFC link. Bandwidth allocation is managed at the CU through an activity status table in each RU and the CU that indicates the status of each timeslot and code assignments. The CU updates the RU tables by downstream messages. Bandwidth can be guaranteed upon request while other services with more bursty traffic may contend for the remainder of the total 10 Mbps payload.

[0035] The advantages over TDMA systems include less need for fast acquisition and correspondingly lower sensitivity to narrowband interference. Further, below a certain SNR, TDMA systems may fail altogether. Contention for certain channels and contention affecting adjacent can cause amplifier overload in TDMA systems and can cause severe throughput and performance problems. FDMA systems where each user gets a narrow upstream frequency slice is very susceptible to narrowband noise which can wipe out an entire channel. FDMA systems often try to avoid this problem with frequency reallocation. This complicates and raises the cost of the system by requiring more intelligence. Throughput is also adversely affected as nothing is sent while frequencies are reallocated. Guardbands between channels waste bandwidth, and frequency misalignment degrades FDMA systems.

[0036] Any method or apparatus that uses these inventive concepts is within the teachings of the invention and is deemed to be equivalent to the apparatus and methods described herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] **FIG. 1** is a block diagram of a bidirectional communication system according to the broadest teachings of the invention.

[0038] **FIG. 2A** is a diagram of typical upstream or downstream fram structure showing how each frame is separated from its neighbors by a gap.

[0039] **FIG. 2B** is a time diagram illustrating how the general ranging process works.

[0040] **FIG. 3** is a time diagram which illustrates a problem which can occur when the network expands.

[0041] **FIG. 4** is a time diagram which illustrates how the problem illustrated in **FIG. 3** can be solved in one embodiment.

[0042] **FIGS. 5A through 5C** are a flow chart of a general ranging process according to one embodiment.

[0043] **FIG. 6** is a flow chart illustrating one embodiment of how re-synchronization to frame boundaries can be achieved by dead reckoning after the CU changes its delay vector.

[0044] **FIG. 7** is a flow chart illustrating another embodiment of how re-synchronization to frame boundaries can be achieved by a downstream instruction from the CU after the CU changes its delay vector.

[0045] **FIG. 8** is a block diagram of an RU modem according to one embodiment of the invention.

[0046] **FIG. 9** is a block diagram of a framer circuit for use in the CU and RU transmitter sections.

[0047] **FIG. 10** is a timing diagram illustrating the relationships of various clock signals in one embodiment of the system.

[0048] **FIG. 11** is a block diagram of a timebase PLL circuit for use in generating the master clock in the CU or recovering the master clock from a clock steering signal from the frame detector in the RU.

[0049] **FIG. 12** is a diagram of the timing offset relationship between the receiver frame counter and the transmit frame counter in the RUs for purposes of achieving frame synchronization.

[0050] **FIG. 13** is a diagram of how the transmit frame timing delay translates to the state of fill of memory in the framer circuit.

[0051] **FIG. 14** is a diagram illustrating the interleaving of data in the framer circuit and how the framer circuit is emptied for transmission.

[0093] **FIG. 55** is a block diagram of a simple CU SCDMA receiver with no tracking loops for clock and carrier synchronization with the RUs.

[0094] **FIG. 56** is a block diagram of a simple RU SCDMA, FFT^{-1} or DMT transmitter.

[0095] **FIG. 57** is a block diagram of a simple bidirectional digital data communication system which uses TDMA or any other multiplexing scheme for downstream transmission and synchronous TDMA for upstream transmission.

[0096] **FIG. 58** shows a diagram of the ranging registers as a function of timing offset.

[0097] **FIG. 59** is a simple block diagram of the hardware involved in the equalization structure of the RUs used in the equalization training process of the preferred embodiment.

[0098] **FIG. 60** is a flow chart of the preferred 2-step initial equalization training process.

[0099] **FIG. 61** is a flow chart of the preferred equalization training stability check process.

[0100] **FIG. 62** is a flow diagram of the preferred periodic 2-step equalization training process.

[0101] **FIG. 63** is a flow diagram of the preferred rotational amplifier correction process to insure that the rotational amplifier has not falsely locked on a local minima.

[0102] **FIG. 64** is a flow diagram of the preferred equalization convergence check.

[0103] **FIG. 65** is a flow diagram of the preferred power alignment process.

[0104] **FIG. 66** is a network diagram showing a typical installation of a distributed system wherein the teachings of the invention are useful.

[0105] **FIG. 67** is a diagram showing how the offset register affect the frame number count in the transmitter of RUs in boundless ranging systems.

[0106] **FIG. 68** is a ranging timing diagram for an alternative form of ranging.

[0107] **FIG. 69** is a ranging timing diagram for a distributed system having a maximum TTA of 3 frames.

[0108] **FIG. 70** illustrates a 6 chip wide ranging listening window in a gap.

[0109] **FIG. 71** illustrates how 6 contention vectors V1 through V6 are generated from the 6 chips of the listening window of 32 consecutive frames to find contentions or valid IDs.

[0110] **FIG. 72** is a table showing 8 valid IDs arranged on the 8 chips of an 8 chip listening window of 33 consecutive frames, and showing no contentions.

DETAILED DESCRIPTION OF THE PREFERRED AND ALTERNATIVE EMBODIMENTS

[0111] Referring to **FIG. 1**, there is shown a block diagram of a bidirectional, digital, passband communication system employing the teachings of the invention. The circuits to the left of doffed line **10** represent the central unit modem or transceiver, while circuits to the right of dotted line **10** represent the remote unit modem or transceiver. A message source **12** provides a downstream message signal on line **14** which may be either digital or analog. This signal is received and encoded by an encoder **16** which may be any type of encoder/multiplexer known in the prior art or later developed. The encoder **16** receives a master clock signal on bus **22** from master clock oscillator **24**. The master clock signal on line **22** will be the clock signal to which the entire system synchronizes. The master clock signal defines the bit times or chip times during which a single bit or symbol comprised of multiple bits are used by modulator **20** to modulate the phase, amplitude or frequency of the master carrier signal which the modulator receives on line **26** from a master carrier synthesizer **28**. The function of the encoder, among other things, is to assemble bits from the message source **12** into the groups which define each symbol which is to be transmitted during each chip time defined by the master clock (where a symbol could be a single binary bit), to assemble the chips into frames and to generate the framing signal which marks the frame boundaries. If a multiplexed system exists, the encoder **16** assembles the data to be transmitted on each virtual channel and prepares the data for multiplexing. In the case of code division multiple access or time division multiple access systems, the encoder **16** does the actual multiplexing of data from different sources onto different codes or into different timeslots on bus **18** and generates the frame boundary markers. If a frequency division multiplexed system is in use, the encoder **16** assembles the different data streams to be transmitted on the different frequencies and outputs them on separate buses represented by line **18** to the modulator **20** and generates frame boundary markers. The modulator **20** receives multiple carriers, all phase coherent with the master carrier from the master carrier synthesizer **28**, and modulates each data stream onto its own dedicated carrier.

[0112] If the signal on line **14** from the message source **12** is analog, one of the functions of the encoder **16** is to sample and digitize it prior to assembly of the digital data into symbols or chips to be transmitted during each chip or bit time.

[0113] If message source **12**, is digital, it emits one symbol every T seconds with the symbols belonging to an alphabet of M symbols comprised of symbols m_1, m_2. . . . In binary systems, there are only two symbols, logic 1 and logic 0. In larger alphabets, each symbol may be represented by multiple bits so the output on line **14** is M-ary meaning there are M possible symbols in the alphabet, each of which can be made up of multiple bits. Generally, encoder **16** serves to produce a signal vector S made up of N elements with one such set for each of the M symbols in the source alphabet.

[0114] The signal vector S is passed on bus **18** to a passband modulator **20**. The details of construction and operation of the modulator **20**, like the details of the construction and operation of the encoder **16** are not critical to the invention, and they can be anything known in the prior art or later developed. The function of the passband modulator **20** is to construct a distinct signal $s_i(t)$ of duration T for each symbol m_i by modulating the master carrier signal during each time T using the bits of the symbol to guide the process of altering the phase, frequency or amplitude or some combination thereof in accordance with the selected modulation scheme.

[0115] Typically, the master clock oscillator **24** is a temperature compensated, crystal controlled oscillator and the clock signal thereof is fed to a master carrier frequency synthesizer **28**, as symbolized by line **30**, for use in synthesis of the master carrier signal. In alternative embodiments, the master carrier synthesizer can be a stand alone crystal controlled oscillator. In other alternative embodiments, the master clock signal need not be generated in the central unit transmitter, and, instead, the master clock signal is received from an external source such as the message source **12**. Likewise, the master carrier can be received from an external source. In still other alternative embodiments, the master clock and master carrier synthesizer need not be crystal controlled and may even vary in frequency so long as they vary slowly enough that the tracking loops in the remote unit receiver can stay in lock. If variable sources for clock and carrier are used, the periodicity of resynchronization process carried out by a phase detect and adjust circuit **32** in the central unit receiver should be made to have a smaller period so resynchronization is done more frequently. More detail on the function of circuit **32** will be given later.

[0116] After modulation, the signal is transmitted on transmission media **40** to the remote unit or units. Transmission media can be a hybrid fiber coax cable plant, a cellular phone system, a landline telephone network or a local area or wide area network medium connecting computers and peripherals together. Transmission from the central unit to the remote units will be referred to as the downstream direction, while transmission from the remote units to the central unit will be referred to as the upstream direction. The carriers used for upstream and downstream transmission are usually in the RF range of frequencies and are separated in frequency although alternatives discussed below to separate upstream and downstream data may also be used.

[0117] The downstream RF signal is received by both a coherent detector **44** and a carrier and clock recovery circuit **42**. Carrier and clock recovery circuit **42** is typically a phase locked loop or other type tracking loop. The functions of circuit **42** are: to generate a local clock signal and a local carrier signal internally, usually employing voltage controlled oscillators; detect the phase difference between the received master clock signal and the local clock signal and lock the local clock signal in phase and frequency with the received master clock signal and output the phase and frequency locked local clock signal on line **46**; and detect the phase difference between the received master carrier signal and the local carrier signal and lock the phase and frequency of the local carrier signal to the phase and frequency of the received master carrier signal and output the phase and frequency locked local carrier signal on line **48**. The manner in which the master carrier and clock signals are transmitted downstream are not critical to the invention, and any of the ways known in the prior art or later developed will suffice the practice the invention. For example, in multiplexed systems, one code, timeslot or frequency may be devoted solely to sending the master carrier or master clock or both. In the particular example of the invention in a synchronous code division multiplexed environment, the master carrier is sent as a pilot tone on a dedicated code, and the clock information is embedded in a unique Barker code which is transmitted during every guardband between frames of payload data. The details of the construction and operation of PLLs and tracking loops are well known in the art, and any of the prior art configurations that are compatible with the particular manner in which the master carrier and master clock signals are transmitted downstream will suffice to practice the invention. Examples of types of tracking loops other than PLLs that are also known in the prior art for use in carrier synchronization and tracking the phase and frequency of a master carrier are Mth power loops and Costas loops described at page 564-565 of the Haykin treatise incorporated by reference herein. The clock synchronization circuitry in circuit **42** can be as simple as an appropriate filter when the master clock is transmitted with the data bearing signal in multiplexed form. Another approach used in the prior art is to use a noncoherent detector to extract the clock signal embedded in the data. Clock recovery can be performed after carrier recovery to recover the clock from baseband signals output from the coherent detector. The preferred method of clock recovery is to use the early-late gating method to sample the output of a matched filter which has a transfer function matched to a particular signal bearing the clock information such as a unique Barker code or a rectangular clock pulse. Some of the prior art clock synchronization techniques are described at pages 566-7 of the Haykin treatise incorporated by reference herein.

[0118] The coherent demodulator/detector **44** functions to demodulate and detect the incoming symbols and can be any prior art design which is compatible with the modulation scheme used in the central unit transmitter. Although, the detector **44** is stated here to be a coherent detector, in embodiments such as the SCDMA (synchronous code division multiple access) example described below where a rotational amplifier is used to correct phase errors, the demodulator/detector **44** does not have to be coherent. In such embodiments, the demodulator portion does not have to receive a reference carrier which is phase locked with the master carrier so long as the rotational amplifier is used in the detector to correct the resulting phase errors. The same is true for the coherent detector **70** in the CU receiver.

[0119] The function of the demodulator/detector is to use the local carrier reference signal on line **48** to demodulate the payload data from the downstream RF signal, detect the transmitted constellation points and output a baseband signal on line **50**.

[0120] The baseband signal is received and processed by any compatible decoder represented by block **52**. The function of decoder **52** is to reverse the encoding and/or multiplexing process carried out by encoder **16** at the central unit transmitter and determine which symbol was sent during every chip time or bit time. The decoder **52** receives the local clock signal on line **46** and uses it to determine when the bit time or chip time boundaries are for purposes of sampling. The decoder **52** also functions to detect the frame boundaries of the downstream frames and reorganize the received data back into the frames organized by the encoder **16** for output on bus **54**. To assist the decoder is doing the frame boundary recognition, a framing signal is generated on line **55** by a frame detector circuit **57**. Any prior art decoder design that can perform this function for the particular encoding/multiplexing scheme selected for use by the central unit transmitter will suffice to practice the invention. The frame detector circuit **57** receives the downstream RF signal on line **59** (or is coupled to the baseband signal output from the detector **44**) and looks for unique frame boundary signals in the stream of data transmitted from the central unit transmitter. Frame detectors are well known in the art, and there

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is such a circuit in every digital communication system that transmits data in frames. One method of frame detection used in the SCDMA examples presented below is separation of frames by a guardband, and transmission of a unique Barker code by the central unit transmitter during every guardband. This stream of incoming data at the remote receiver is passed through a filter having a transfer function matched to said Barker code and the correlation peak which results when the Barker code passes through the matched filter is used to mark the frame boundaries.

[0121] The upstream payload data is received from any message source **56** on line **58**. An encoder **60** receives this message signal (and digitizes it if necessary) and functions like encoder **16** to assemble the bits into symbols for transmission during each bit time or chip time defined by the local clock reference signal on line **46**. As was the case for encoder **16**, encoder **60** may also do the multiplexing of different channels of data onto different codes or into different timeslots in CDMA or TDMA systems, respectively. In the case of an FDMA system, encoder **60** assembles the message bits from one or more sources into separate bits streams which are supplied to a modulator **62** for use in modulating separate carriers received by the modulator from a synthesizer (not shown) which receives the local carrier reference signal on line **48** and generates a plurality of different carriers therefrom.

[0122] The encoder **60** may use a different form of encoding and/or multiplexing for the upstream direction than were used for the downstream direction. Any encoder design known in the prior art or later developed will suffice for purposes of practicing the invention. In fact, the encoder **60** can even use a clock signal at a different frequency from the master clock signal so long as the different clock signal is phase coherent with the master clock signal. Phase coherent means that there is periodic coincidence in time of clock edges between the two different clock frequencies. In such an embodiment, the local clock reference signal on line **46** (locked in phase and frequency to the master clock) would be supplied to a frequency synthesizer which would then generate the new clock frequency so as to be phase coherent with the master clock signal.

[0123] The upstream data output from the encoder **60** on line **64** is received by an adjustable delay circuit **65** which receives an adjustable delay value Td. This circuit is used when the system of **FIG. 1** requires frame synchronization and the remote units are at differing distances from the central unit. Typically such systems include synchronous TDMA and synchronous CDMA systems. The value of Td is adjusted for each remote unit based upon its physical distance from the central unit so as to achieve frame synchronization. Frame boundaries are delineated by an easily found signal. In frame synchronous systems such as SCDMA, the frame detector **68** can be eliminated.

[0124] The output of the delay circuit **65** is sent to a modulator **62**. Modulator **62** functions to guide modulation of the phase, frequency or amplitude of some combination thereof of one or more carriers. In a single carrier system, the carrier being modulated is the local carrier reference signal on line **48** which is locked in frequency and phase with the master carrier. In an alternative embodiment, the local carrier reference signal is supplied to a frequency synthesizer which generates a different frequency carrier which is phase coherent with master carrier signal. Phase coherent in this context is that there is periodic coincidence in time of zero crossings of the master carrier and the new carrier frequency generated by the synthesizer.

[0125] The particular structure and operation for the passband modulator **62** is not critical to the invention. Also, the particular modulation scheme used is not critical to the invention and need not be the same modulation scheme used in the downstream direction. Any prior art design for a modulator or a design subsequently developed will suffice to practice the invention so long as it is compatible with the type of encoding done by encoder **60**.

[0126] Typically, the transmission in the upstream direction is done at a different frequency from the downstream transmission so as to share the transmission media **40** by frequency division multiplexing. However, other forms of multiplexing such as time division or code division multiplexing may also be used to separate the upstream and downstream data. Frequency translator **66** represents the circuitry needed to separate the downstream and upstream data and it assumes that the form of separation is FDM. If TDMA or CDMA is used to separate the upstream from the downstream data, the circuit **66** represents whatever circuitry is used to do the multiplexing. Such circuitry is well known in the art.

[0127] The upstream RF signal is transmitted across media **40** to a central unit receiver. The upstream RF is coupled in the central unit receiver to a phase detect and adjust circuit **32**, a frame detector **68** and a coherent detector **70**. The function of the phase detect and adjust circuit is: to occasionally or periodically extract the received clock signal and the received carrier signal from the upstream RF signal; determine the phase difference between the extracted clock and carrier signals and the master clock and master carrier signals, respectively; adjust the phase of the master clock and master carrier signals and apply the phase adjusted clock and carrier signals to the decoder **72** and coherent detector **70**, respectively.

[0128] The design of the phase detect and adjust circuit **32** is not critical to the invention, and any circuit that can perform the function stated above will suffice to practice the invention. One example of a phase detect and adjust circuit would be a pair of delay lines through which the master clock and master carrier signals are transmitted, with the amount of delay set to equal the total turnaround time for transmission of the carrier and clock signals from the central unit to the remote unit and back to the central unit. If the total turnaround time is stable, this circuit will adjust the phase of the master clock and master carrier signals for phase coherence with the received clock and carrier signals and once the phase is adjusted, it does not have to be adjusted again. If the total turnaround time changes because of, for example, network expansion, the phase detect portion of the circuit can periodically or occasionally determines the phase differences in any one of a number of different ways known in the prior art. For example, phase differences can be determined by comparing the phase between preamble data and Barker code data encoding the carrier and clock data, respectively, said preamble data and Barker code data being transmitted by each RU occasionally or periodically such as at the beginning of each frame or on a dedicated code or in a dedicated timeslot. The phase information recovered from

ero values and the tap weights nor
additions of those products need be performed.

Detailed Description Text - DETX (9):

The modem receiver 12 essentially performs the inverse operation as the transmitter 10 (FIG. 2). After passage through a analog to digital (A/D) converter 40 the regenerated symbol stream is fed to a demodulator 42 where the x and y signal space coordinates are multiplied by sampled orthogonal carrier sinusoids (e.g. 52.5 kHz) and then fed through low pass filters in demodulator 42. The demodulator 42 also takes advantage of the sample rate being four times the frequency of the carrier signal and the carrier **phase** is adjusted to always be an integer multiple of .pi./2 during each sample time. This avoids having to implement true multiplications since the carrier wave is always at 0, +1, or -1 during the data sampling instant. The x and y coordinate symbol streams are then fed to an adaptive **equalizer 44** to reduce intersymbol interference. A decoder module 46 regenerates the binary data input from the coordinate symbol streams by table look-up using a minimum distance criteria to estimate the most likely received point given the arrival of the equalizer output point during the symbol.

Detailed Description Text - DETX (16):

The overall data transmission rate then varies with the symbol rate and the nu

z sample rate as the transmitter
10. The timing **phase**-locked loop 54 includes bandedge timing filters in order to derive a sample clock signal for driving the A/D converter 40, as well as provide a symbol clock signal.

Detailed Description Text - DETX (70):

The demodulator coordinate outputs are input to adaptive **equalizer 44** at the symbol rate of 70 kHz in order to reduce intersymbol interference. The decoder module 46 takes each of the x and y coordinate streams and produces a decoded digital output stream at a rate corresponding to the specified bit/symbol packing density using a table look-up procedure. Error signals are also derived from the decoding operation in order to update the taps of adaptive **equalizer 44**. Finally, the data is unscrambled by descrambler 56 as shown in FIGS. 2 and 7 to produce the original baseband input signal.

Detailed Description Text - DETX (76):

FIG. 10 is a flow diagram of the control logic of the primary state machine. This 8 state machine selects the basic operating mode of the transmitter 10: OFF (no signal), TONE (for carrier frequency acquisition), TWO-POINT (for carr